I claim:

1. A method for driving a semiconductor switch having load current limiting and thermal protection, a maximum load current being limited and the semiconductor switch switching off upon a predetermined upper temperature being exceeded and switching on again when a chip temperature falls below a predetermined lower temperature, which comprises the steps of:

operating the semiconductor switch in one of a normal mode and a fault mode;

operating the semiconductor switch in the fault mode upon exceeding the predetermined upper temperature; and

limiting a load current to a first maximum value in the normal mode and to a second maximum value, being lower than the first maximum value, in the fault mode.

2. The method according to claim 1, which further comprises switching on the semiconductor switch when the chip temperature falls below the predetermined lower temperature in the normal mode and in the fault mode.

3. The method according to claim 1, which further comprises switching off the semiconductor switch, when in the fault mode, if a further upper temperature is exceeded, the further

upper temperature is lower than the predetermined upper temperature.

4. The method according to claim 1, which further comprises limiting the load current by actuating the semiconductor activating switch.

5. The method according to claim 1, which further comprises:

monitoring a voltage across a load path of the semiconductor switch; and

operating the semiconductor switch in the normal mode when a load path voltage is smaller than a predetermined threshold value.

6. A circuit configuration, comprising:

a semiconductor switch having a drive terminal and a load path;

a protective circuit connected to said drive terminal of said semiconductor switch;

a temperature sensor disposed in a region of said semiconductor switch and coupled to said protective circuit,

said temeprature sensor providing a temperature measuring signal fed to said protective circuit; and

a current measuring configuration coupled to said protective circuit and generating a current measuring signal being dependent on a current across said load path of said semiconductor switch;

said protective circuit storing first and second overcurrent signals, said protective circuit assuming one of a first operating mode and a second operating mode, and, depending on a mode, said protective circuit controling said semiconductor switch according to a comparison of the current measuring signal to the first overcurrent signal or according to a comparison of the current measuring signal to the second overcurrent signal.

7. The circuit configuration according to claim 6, wherein said protective circuit stores first and second overtemperature signals, and, depending on the mode, said protective circuit drives said semiconductor switch into a blocking state according to a comparison of the temperature measuring signal to the first overtemperature signal or according to a comparison of the temperature measuring signal to the second overtemperature signal.

8. The circuit configuration according to claim 6, further comprising a voltage measuring configuration for detecting a load path voltage of said semiconductor switch and connected to said protective circuit, said voltage measuring configuration providing a voltage measuring signal that is fed to said protective circuit, said protective circuit assumes one of the first and second modes depending on the voltage measuring signal.